

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)			ATTY. DOCKET NO. 43876-158		SERIAL NO. Continuation of Serial No. 10/646,787	
			APPLICANT HANSEN, et al.			
			FILING DATE January 16, 2004		GROUP To be assigned	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,025,772	05/24/77	Constant			
	4,489,393	12/18/84	Kawahara, et al.			
	4,701,875	10/20/87	Konishi, et al.			
	4,727,505	02/23/88	Konishi, et al.			
	4,876,660	10/24/89	Owens, et al.			
	4,893,267	01/09/90	Alsup, et al.			
	4,956,801	09/11/90	Priem et al.			
	4,969,118	11/06/90	Montoye, et al.			
	4,975,868	12/04/90	Freerksen			
	5,032,865	07/16/91	Schlunt			
	5,157,388	10/20/92	Kohn			
	5,201,056	04/06/93	Daniel, et al.			
	5,268,855	12/07/93	Mason, et al.			
	5,268,995	12/07/93	Diefendorff, et al.			

FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						<input type="checkbox"/> Yes <input type="checkbox"/> No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987
	Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen, IEEE Micro. April 1992, 40-63
	Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.
	IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, Microprocessor Report July 31, 1995, 15-16

EXAMINER	DATE CONSIDERED 4/11/06
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125	5,408,581	04/18/95	Suzuki, et al.			
	5,423,051	06/06/95	Fuller, et al.			
	5,426,600	06/20/95	Nakagawa, et al.			
	5,500,811	03/19/96	Corry			
	5,557,724	09/17/96	Sampat, et al.			
	5,588,152	12/24/96	Dapp, et al.			
	5,592,405	01/07/97	Gove, et al.			
	5,640,543	06/17/97	Farrell, et al.			
	5,642,306	06/24/97	Mennemeier, et al.			
	5,666,298	09/09/97	Peleg, et al.			
	5,669,010	09/16/97	Duluk, Jr.			
	5,673,407	09/30/97	Poland, et al.			
	5,675,526	10/07/97	Peleg, et al.			
125	5,680,338	10/21/97	Agarwal, et al.			

FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
125	0 474 246 A2	06/09/91	EP				
125	0 654 733 A1	05/07/94	EP				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
125	The Visual Instruction Set (VIS) in UltraSPAR™, L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, IEEE, May 3, 1995, 462-469 Osborne McGraw-Hill, i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn, 1990, 8-10; 171-175; 182-183
125	A General-Purpose Array Processor for Seismic Processing, Nov-Dec., 1984, Volume 1, No. 3) Revisiting past digital signal processor technology, Don Shaver- Jan-Mar. 1998, 5-26
125	Ruby B. Lee, "Accelerating Multimedia with Enhanced Microprocessors", IEEE Micro, April 1995, 22-32.

EXAMINER <i>Key 2</i>	DATE CONSIDERED <i>4/11/06</i>
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WDC99 864144-1.043876.0158

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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	5,721,892	02/24/98	Peleg, et al.				
	5,734,874	03/31/98	Van Hook, et al.				
	5,757,432	05/26/98	Dulong, et al.				
	5,758,176	05/26/98	Agarwal, et al.				
	5,802,336	09/01/98	Peleg, et al.				
	5,809,292	09/15/98	Wilkinson, et al.				
	5,818,739	10/06/98	Peleg, et al.				
	5,825,677	10/20/98	Agarwal, et al.				
	5,835,782	11/10/98	Chu Lin, et al.				
	5,886,732	03/23/99	Humpleman				
	5,922,066	07/13/99	Cho, et al.				
	5,983,257	11/09/99	Dulong, et al.				
	6,016,538	01/18/00	Guttag, et al.				
	6,092,094	07/18/00	Ireton				
	6,401,194 B1	06/04/02	Nguyen, et al.				
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**Continuation of Serial No.
10/646,787**

APPLICANT
Craig HANSEN, et al.

(PTO-1449)

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GROUP
To be assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
A		US 4,785,393	11/15/1988	Chu et al.	
		US 4,814,976	03/21/1989	Craig C. Hansen, et al.	
		US 5,031,135	07/09/1991	Patel	
		US 5,280,598	01/1994	Osaki et al.	
		US 5,481,688	01/02/1996	Dockser	
		US 5,487,024	01/1996	Girardeau Jr.	
		US 5,600,814	02/1997	Gahan et al.	
		US 5,740,093	04/14/1998	Sharangpani	
		US 5,742,840	04/21/1998	Hansen et al.	
		US 5,768,546	06/1998	Kwon	
		US 5,898,849	04/27/1999	Tran	
		US 5,996,057	11/30/1999	Hunter L. Scales, III, et al.	
		US 6,041,404	03/21/2000	Patrice Roussel, et al.	
		US 6,052,769	04/18/2000	Thomas R. Huff, et al.	
		US 6,173,393 B1	01/09/2001	Salvador Palanca, et al.	
		US 6,275,834 B1	08/14/2001	Derrick Chu Lin, et al.	
		US 6,295,599	09/2001	Hansen et al.	

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						Yes	No

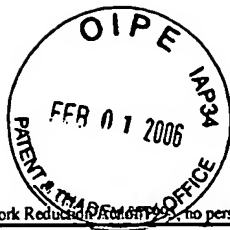
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
H		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)
H		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).
		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).
		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).
EXAMINER		DATE CONSIDERED
4/11/06		

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PTO/SB/08a 07-05)

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/757,925
				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	1	of	10	Attorney Docket Number	43876-158

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
12	AA	US-4,852,098	07/25/1989	Brechard, et al.	
	AB	US-4,875,161	10/17/1989	Lahti, et al.	
	AC	US-4,949,294	08/14/1990	Wambergue, et al.	
	AD	US-4,953,073	08/28/1990	Moussouris, et al.	
	AE	US-4,959,779	09/25/1990	Weber, et al.	
	AF	US-5,081,698	01/14/1992	Kohn	
	AG	US-5,113,506	05/12/1992	Moussouris, et al.	
	AH	US-5,155,816	10/13/1992	Kohn	
	AI	US-5,161,247	11/03/1992	Murakami, et al.	
	AJ	US-5,179,651	01/12/1993	Taaffe, et al.	
	AK	US-5,231,646	07/27/1993	Heath, et al.	
	AL	US-5,233,690	08/03/1993	Sherlock, et al.	
	AM	US-5,241,636	08/31/1993	Kohn	
	AN	US-5,280,598	01/18/1994	Osaki, et al.	
	AO	US-5,487,024	01/23/1996	Girardeau, Jr.	
	AP	US-5,515,520	05/07/1996	Hatta, et al.	
	AQ	US-5,533,185	07/02/1996	Lentz, et al.	
	AR	US-5,590,365	12/31/1996	Ide, et al.	
	AS	US-5,600,814	02/04/1997	Gahan, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
15	AT	WO 93/11500				
Examiner Signature				Date Considered	4/11/06	

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				Application Number	10/757,925	
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				First Named Inventor	Craig C. HANSEN, et al.	
				Group Art Unit	2183	
Examiner Name	CHAN, EDDIE P					
Attorney Docket Number	43876-158					
Sheet	2	of	10			

OTHER PRIOR ART – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T ²
H	AU	IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)	
	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)	
	AW	Gery Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 – 848)	
	AX	IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767)	
	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228)	
	AZ	MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621)	
	BA	i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn	
	BB	Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900)	
	BC	Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455)	
	BD	Gutttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, pp. 53-64 (November 1992) (51056DOC000913 – 924)	
	BE	Lee et al., "MediaStation 5000: Integrating Video and Audio," IEEE Multimedia pp. 50-61 (Summer 1994) (51056DOC000901 – 912)	
	BF	TMS320C80 (MVP) Parallel Processor User's Guide, Texas Instruments (March 1995) (51056DOC003744 – 4437)	
	BG	TMS320C80 (MVP) Master Processor User's Guide, Texas Instruments (March 1995) (51056DOC000925 – 957)	
	BH	Bass et al., "The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 12-22 (April 1995) (51056DOC059283 – 289)	
	BI	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard Journal, Vol. 46, No. 2, p. 79 (April 1995) (51056DOC059277 – 282)	
BJ	Gwennap, "New PA-RISC Processor Decodes MPEG Video: Hewlett-Packard's PA-7100LC Uses New Instructions to Eliminate Decoder Chip," Microprocessor Report, pp. 16-17 (January 24, 1994) (51056DOC002140 – 141)		
BK	Gwennap, "Digital MIPS Add Multimedia Extensions," Microdesign Resources, pp. 24-28 (November 18, 1996) (51056DOC003454 – 459)		
BL	Kurpanck et al., "PA7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," IEEE COMPCON '94, pp. 375-82 (February 28- March 4, 1994) (51056DOC002149 – 156)		
BM	Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC068161 – 167)		
BN	Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557)		

Examiner Signature	<i>[Signature]</i>	Dated Considered	4/11/06
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12	BO	US-5,636,351	06/03/1997	Lee	
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	BR	US-5,758,176	05/26/1998	Agarwal, et al.	
	BS	US-5,768,546	06/16/1998	Kwon	
	BT	US-5,887,183	03/23/1999	Agarwal, et al.	
	BU	US-5,996,057	11/30/1999	Scales III, et al.	
	BV	US-6,425,073	07/23/2002	Roussel, et al.	
	BW	US-6,516,406	02/04/2003	Peleg, et al.	
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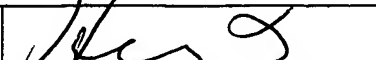
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1/5	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 - 351)	
	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 - 090)	
	BZ	Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 - 590)	
	CA	HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 - 141)	
	CB	PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 - 176)	
	CC	Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 - 776)	
	CD	Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 - 519)	
	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 - 751)	
	CF	Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 - 763)	
	CG	Nikhil et al., "*T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 - 476)	
	CH	Papadopoulos et al., "*T: Integrated Building Blocks for Parallel Computing," ACM, pp. 624-35 (1993) (51056DOC007278 - 289)	
	CI	Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC0069260 - 262)	
	CJ	M. Phillip, "Performance Issues for 88110 RISC Microprocessor," IEEE, 1992 (51056DOC008752 - 757)	
	CK	M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 - 789)	
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	CM	J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 - 742)	
	CN	K. Pepe, "The MC88110's High Performance Load/Store Unit," Northcon, 1992 (51056DOC009743 - 747)	
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	CP	Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 - 646)	
	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 - 661)	
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Examiner Signature		Dated Considered	4/11/06
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Substitute for form I449B/PTO		Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/757,925	
		Filing Date	January 16, 2004	
		First Named Inventor	Craig C. HANSEN, et al.	
		Group Art Unit	2183	
		Examiner Name	CHAN, EDDIE P	
Sheet	5	of	10	
		Attorney Docket Number	43876-158	
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS); title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T ²	
	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 - 194)		
	CV	Broughton et al., "The S-I Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 - 607)		
	CW	Farmwald et al., "Signal Processing Aspects of the S-I Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)		
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034)		
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 - 279)		
	CZ	Widdoes, "The S-I Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)		
	DA	Cornell, S-I Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)		
	DB	The S-I Project, January 1985, S-I Technical Staff (51056DOC057368 - 607)		
	DC	S-I Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 - 918)		
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)		
	DE	Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618)		
	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)		
	DG	Satum Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)		
	DH	Satum Differences from C Series (February 6, 1994) (51056DOC017150 - 157)		
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)		
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)		
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)		
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)		
	DM	Satum Overview (November 12, 1993) (51056DOC017111 - 157)		
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 - 7510)		
DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)			
DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 - 443)			
DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 - 459)			
DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 - 5299)			
DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)			
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Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/757 925
		Filing Date	January 16, 2004
		First Named Inventor	Craig C. HANSEN, et al.
		Group Art Unit	2183
		Examiner Name	CHAN, EDDIE P
Sheet	6	of	10
		Attorney Docket Number	43876-158
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T ²
DT	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
DU	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
DV	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 - 666)	
DW	DW	Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. 1, pp. 275-84 (April 17-20, 1989) (5156DOC070711 - 717)	
DX	DX	Grimes et al., "The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities," IEEE Computer Graphics & Applications, pp. 85-94 (July 1989) (5156DOC070701 - 710)	
DY	DY	Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 - 094)	
DZ	DZ	Kohn et al., "A New Microprocessor with Vector Processing Capabilities," Electro/89 Conference Record, pp. 1-6 (April 11-13, 1989) (5156DOC070672 - 678)	
EA	EA	Kohn et al., "Introducing the Intel i860 64-Bit Microprocessor," IEEE Micro, pp. 15-30 (August 1989) (5156DOC070627 - 642)	
EB	EB	Kohn et al., "The i860 64-Bit Supercomputing Microprocessor," AMC, pp. 450-56 (1989) (51056DOC000330 - 336)	
EC	EC	Margulis, "i860 Microprocessor Architecture," Intel Corporation (1990) (51056DOC066610 - 7265 and 5156DOC069971 - 70626)	
ED	ED	Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 - 700)	
EE	EE	Patel et al., "Architectural Features of the i860 - Microprocessor RISC Core and On-Chip Caches," IEEE, pp. 385-90 (1989) (5156DOC070679 - 684)	
EF	EF	Rhodchamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 - 647)	
EG	EG	Perry, "Intel's Secret is Out," IEEE Spectrum, pp. 22-28 (April 1989) (5156DOC070648 - 654)	
EH	EH	Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 - 101)	
EI	EI	i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 - 427)	
EJ	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 - 9097)	
EK	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
EL	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
EM	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
EN	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
EO	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	
EP	EP	N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 - 73027)	
EQ	EQ	Hansen, "Architecture of a Broadband MediaProcessor," IEEE COMPCON 96 (February 25-29, 1996) (MU0013276 - 283 and 51057DOC001825 - 831)	
ER	ER	Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 - 630)	
Examiner Signature			Dated Considered
			4/11/04

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				Application Number	10/757,925
				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	7	of	10	Attorney Docket Number	43876-158

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
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[Handwritten mark]	ES	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958)		
	ET	Bell, "Ultracomputers: A Teraflo Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 – 923)		
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 – 040)		
	EV	Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 – 300)		
	EW	Donovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 – 645)		
	EX	Fields, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin-Madison, http://www.cs.wisc.edu/condor/doc/WiscIdea.html (1993) (51056DOC068704 – 711)		
	EY	Geist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 – 929)		
	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 – 705)		
	FA	Giloi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 – 801)		
	FB	Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 – 673)		
	FC	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 – 662)		
	FD	Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 – 1028)		
	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 – 694)		
	FF	Jain et al., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEE ICASSP '94, pp. II-521 – II-524 (April 1994) (51056DOC003070 – 073)		
	FG	Laudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 – 327)		
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 – 942)		
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 – 699)		
	FJ	Litzkow et al., "Condor – A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 – 719)		
FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 – 628)			
FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 – 471)			
FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 – 942)			
Examiner Signature	[Handwritten Signature]		Dated Considered	4/11/06

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				Application Number	10/757,925
				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	8	of	10	Attorney Docket Number	43876-158

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS				
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125	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 - 948)		
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 - 887)		
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110-118) (51056DOC002949 - 957)		
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 - 896)		
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)		
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 - 946)		
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 - 609)		
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)		
	FV	Toyokura et al., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipelined Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.5, pp. 74-75 (1994) (51056DOC003659 - 660)		
	FW	Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 - 443)		
	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 - 256)		
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 - 936)		
	FZ	Wang, "Bit-Level Systolic Array for Fast Exponentiation in GF(2m)," IEEE Transactions on Computers, Vol. 43, No. 7, pp. 838-41 (July 1994) (51056DOC059407 - 410)		
	GA	Ware et al., "64 Bit Monolithic Floating Point Processors," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC059646 - 655)		
	GB	"Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206)		
	GC	Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209)		
	GD	Data General AViiON AV500, 550, 4500 and 5500 Servers		
	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)		
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)		
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 - 243)		
125	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)		

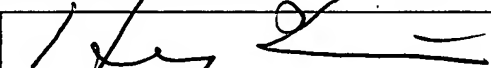
Examiner Signature		Dated Considered	4/11/06
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T ²
	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)	
		Original Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	
	GJ	Amended Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	
	GK	Expert Witness Report of Richard A. Killworth, Esq., <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	
	GP	Request for <i>Inter Partes</i> Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	
	GQ	Deposition of Larry Menneimer on September 22, 2005 and Exhibit 501; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GR	Deposition of Leslie Kohn on September 22, 2005; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GS	Intel Article, "Intel Announces Record Revenue of 9.96 Billion", October 18, 2005	
	GT	The New York Times Article, "Intel Posts 5% Profit Increase on Demand for Notebook Chips", October 19, 2005	
	GU	USA Today Article, "Intel's Revenue Grew 18% In Robust Quarter for Tech", October 19, 2005	
	GV	The Wall Street Journal Article, "Intel Says Chip Demand May Slow", October 19, 2005	
	GW	The New York Times Article, "Intel Settlement Revives A Fading Chip Designer", October 20, 2005	

Examiner Signature		Dated Considered	4/11/06
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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 043876-0158		SERIAL NO. 10/757,925	
				APPLICANT Craig HANSEN, et al.			
				FILING DATE January 16, 2004		GROUP 2183	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	A	US 6,643,765	11-04-2003	Hansen et al.		
	B	US 6,725,356	04-20-2004	Hansen et al.		
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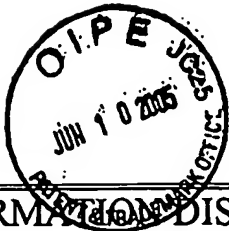
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
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	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)	
	D	Intel Press Release, "Intel Announces Record Revenue of \$9.96 Billion," Santa Clara, CA, 10-18-2005	

EXAMINER 	DATE CONSIDERED 1/11/06
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SHEET 1 OF 11

INFORMATION DISCLOSURE
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APPLICATION

(PTO-1449)

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		US 4,875,161	10/17/1989	Lahti	
		US 4,949,294	08/14/1990	Wambergue	
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		US 4,959,779	09/25/1990	Weber et al.	
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		US 6,657,908 B1	05/20/2003	Furuhashi	

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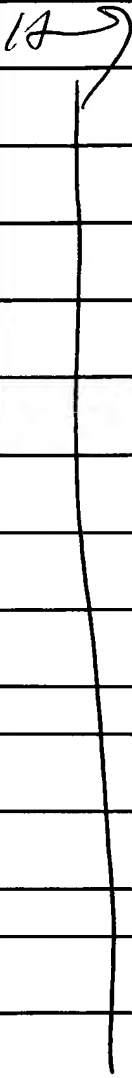
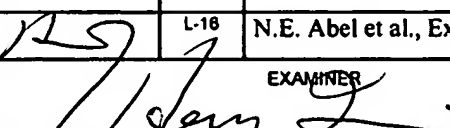
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						Yes	No
125		JP 3268024	11/28/1991	Hitachi Ltd.			
		EP 0 468 820 A2	01/29/1992	Fujitsu Limited			
		WO 93/01565	01/21/1993	Seiko Epson Corporation			
		CA 1 323 451	10/19/1993	Northern Telecom Ltd.			
		JP 6095843	04/08/1994	IBM			
		EP 0 651 321 A	05/03/1995	Advanced Micro Devices Inc.			
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		JP-S60-217435	10/31/1985	Toshiba Corp.			
		WO 97/07450	02/27/1997	Microunity Systems Engineering, Inc.			

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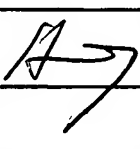

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)		ATTY. DOCKET NO. 043876-0158	SERIAL NO. 10/757,925
		APPLICANT HANSEN, C., et al.	
		FILING DATE January 16, 2004	GROUP 2183
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
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	L-1	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," p. 12-21, 28 March 1993, IEEE J. OF SOLID-STATE CIRCUITS.	
	L-2	K. Uchiyama et al., The Gmicro/500 Superscalar Microprocessor with. Branch Buffers, IEEE Micro, October 1993, p. 12-21.	
	L-3	Ruby B. Lee, Realtime MPEG Video Via Software Decompression on a PA-RISC Processor, IEEE (1995).	
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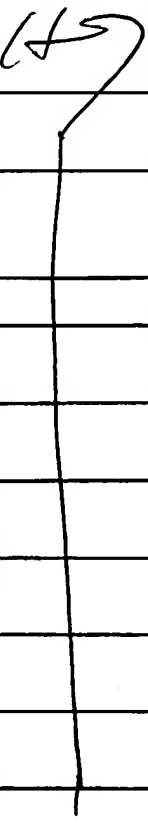


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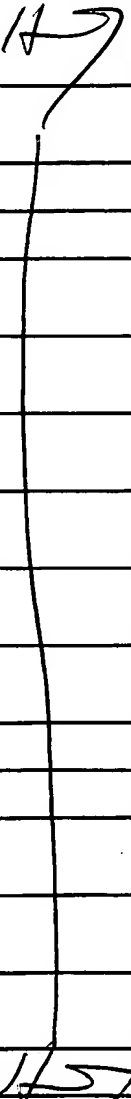

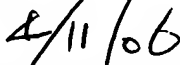
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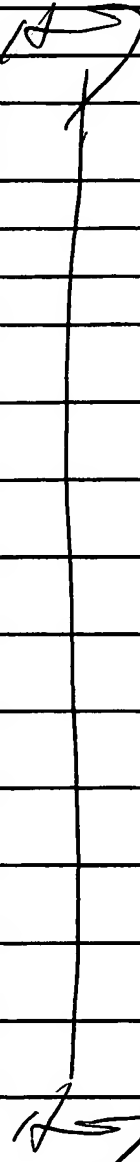

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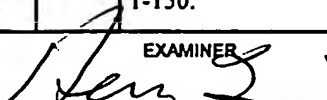
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		FILING DATE January 16, 2004	GROUP 2183
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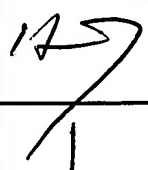
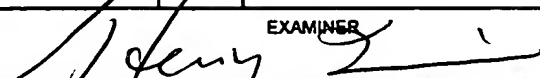
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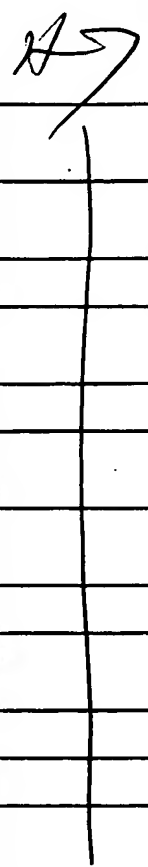
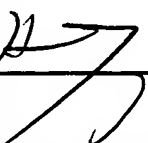

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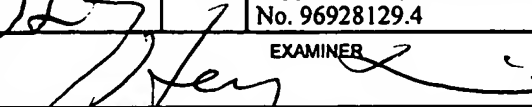
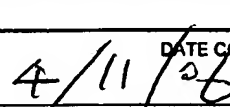
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